REMARKS

Claims 1-2, 4-13 and 15-17 remain in the present application. Applicant respectfully requests further examination and reconsideration of the rejections based on the amendments and arguments set forth below.

Allowable Subject Matter

Applicant would like to thank the Examiner for the indication that Claims 16-17 are allowed.

Claim Rejections – 35 U.S.C. §103

Claims 1-2, 4-13 and 15 are rejected in the present Office Action under 35 U.S.C. §103(a) as being unpatentable over United States Patent Number 6,173,419 to Barnett (hereafter referred to as "Barnett"), in view of United States Patent Number 6,061,511 to Marantz et al. (hereafter referred to as "Marantz"). Applicant has reviewed the cited references and respectfully submits that the embodiments of the present invention as recited in Claims 1-2, 4-13 and 15 are not rendered obvious by Barnett in view of Marantz for the following reasons.

Applicant respectfully directs the Examiner to independent Claim 1 that recites a method of obtaining debug information comprising (emphasis added):

> executing a sequence of instructions by a device under test (DUT), wherein said DUT comprises a data line and a clock line;
> executing the sequence of instructions by an emulator device emulating the functions of the DUT and executing the sequence of instructions in lock-step fashion with the DUT, wherein said emulator device shares a clock signal with said DUT;
> the DUT conveying I/O read information to the emulator device over said data line during a data transfer phase; and
> a host computer system reading real-time state and debug information from the emulator device without interrupting the DUT.

Independent Claim 9 recites limitations similar to those in independent Claim 1. Claims 2, 4-8, 10-13 and 15 depend from independent Claims 1 and 9, and recite further limitations to the claimed invention.

Applicant respectfully submits that Barnett fails to teach or suggest the limitations of "wherein said emulator device shares a clock signal with said DUT" as recited in independent Claim 1. As recited and described in the present application, an emulator device emulates the functions of a device under test (DUT), wherein both the emulator device and DUT share a clock signal (page 15, lines 16-22 of the present application), and therefore, are commonly clocked in operation.

In contrast to the claimed embodiments, Applicant understands Barnett to teach an emulation system where an FPGA does *not* and *cannot* share a common clock signal with a target CPU. Specifically, Barnett teaches on line 64 of column 6 through line 2 of column 7 that "the emulator programmed into the FPGA is identical to the target CPU IC logic but not in timing... [t]he FPGA is not able to handle the timing and asynchronous signals of the signals on the pins of a target CPU." As such, Applicant respectfully submits that Barnett teaches away from the claimed embodiments by teaching that an FPGA and target CPU do *not* share a common clock signal in contrast to the claimed emulator device and the claimed DUT sharing a common clock signal.

Applicant respectfully submits that Marantz, either alone or in combination with Barnett, also fails to teach or suggest the limitations of "wherein said emulator device shares a clock signal with said DUT" as recited in independent Claim 1. In contrast to the claimed embodiments, Applicant understands

Marantz to teach an emulator that is "discretized to a "virtual clock" (vclk) signal, which is typically many times the frequency of the clock signals of the design under emulation" (col. 1, lines 52-55). As such, assuming arguendo that a design under emulation as taught by Marantz is analogous to a DUT as claimed, Applicant respectfully submits that Marantz teaches away from the claimed embodiments by teaching that an emulator does not share a clock signal with a DUT instead of an emulator device and a DUT sharing a clock signal as claimed.

For these reasons, Applicant respectfully submits that independent Claim 1 is not rendered obvious by Barnett in view of Marantz, thereby overcoming the 35 U.S.C. §103(a) rejection of record. Since independent Claim 9 contains limitations similar to those discussed above with respect to independent Claim 1, independent Claim 9 also overcomes the 35 U.S.C. §103(a) rejections of record. Since dependent Claims 2, 4-8, 10-13 and 15 recite further limitations to the invention claimed in their respective independent Claims, Claims 2, 4-8, 10-13 and 15 are also not rendered obvious by Barnett in view of Marantz. Therefore, Claims 1-2, 4-13 and 15 are allowable.

CONCLUSION

Applicant respectfully submits that Claims 1-2, 4-13 and 15-17 are in condition for allowance and Applicant earnestly solicits such action from the Examiner.

The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

WAGNER, MURABITO & HAO, LLP

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BMF

Bryan M. Failing
Registration No. 57,974

Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060